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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,533	04/08/2004	Arunangshu Kundu	ACT-299COA	1284

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,533	KUNDU ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claim 1 is presented for examination.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,751,723. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons :

3. Although the patented claim 1 did not recite the system bus connected to output of the field programmable gate array virtual component interface translator to the outputs of the microcontroller virtual component interface translator as recited in current claim 1, it would have been obvious to one of ordinary skill in the art to include the system bus connecting the outputs of the field programmable gate array virtual component interface translator and the microcontroller virtual component interface translator because patented claim 1 already taght the connection of the system bus with

the microcontroller virtual component interface translator to receive signal from the field programmable gate array core (see patented claim 1, lines 25-29) and the connection of the system bus to the field programmable gate array virtual component interface translator (see patented claim , lines 21-24), therefore, the system bus was a common bus connection to both the field programmable gate array virtual component interface translator and the microcontroller virtual component interface translator, and therefore, the output connections between the field programmable gate array virtual component interface translator and the microcontroller virtual component interface translator on the given system bus was applicable to achieve the sharable interface of the two interface translators, and in doing so, provided a motivation.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meyer et al. (5,896,414) in view of van der Wal et al. (6,188,381)

5. As to claim 1, the functional operations of the "virtual component interface translator" (line 4) and the field programmable gate array translator" (line 8) are not reflected in the claim, and only the output and input connections are recited in the claim. According to the applicant specification (page 6, lines 11-19), the virtual component interface translator was used to translate component signals into universal or standard protocol signals . Therefore, it is assumed any encoder or translator which converts signals into standardized signals in a FPGA system will read on the claim language. Applicant is suggested to clarify the functional use of these two elements in the claim in the next response.

6. Meyer disclosed a data processing system (see fig.5, see fig.2 for overall diagram) including at least :

a) a field programmable gate array [FPGA 506] core having logic clusters (see the flash ROM and the static RAM connected therein), static ram [504], and routing resources (see the interface write and select ;

b) field programmable gate array component interface bus having inputs and outputs connected to the field programmable gate array (e.g. see the FPGA data bus in fig.5);

c)a micro controller [micro controller 500] (fig.5);

d) micro controller virtual component interface translator [MOD][[DEMOD] having inputs and outputs connected to the micro controller (see the micro controller bus connections to the MOD and DEMODs in fig.5);

e) data bus connected to the outputs of the field programmable gate array virtual component interface bus [FPGA data bus] to the outputs of the micro controller virtual components interface data bus (see the Micro controller data bus in fig.5).

f) direct connection between micro controller [500] to the routing resources of the FPGA (see fig.5 [flash ROM 502][Static RAM 504]).

7. Meyer did not specifically teach the "virtual component interface translator" having output and input connected to the FPGA as claimed. Instead , Meyer taught a general data bus having input and output connections to the FPGA core (see fig.5). However, van der Wal disclosed a system including interface translator having input

and output connections to FPGA for translating component signals into a standard signal (e.g. see col.28, lines 32-39, see also fig.8, and col.28, lines 56-67, col.29, lines 1-5, col.30, lines 1-37 for the background of input and output connections to the FPGA). It would have been obvious to one of ordinary skill in the art to include the virtual component interface translator having input and output to the FPGA as claimed because the use of van del Wal could provide enhanced control capability of the micro controller in Meyer to adapt to a predefined set of hardware components (e.g. different type of peripheral devices,) at a single standardized signal format, and thereby minimizing the circuit overheads, and it could be readily achieved by predefining the configuration parameters (e.g. the bit format, and length) of translator of van der Wal into Meyer such that the conversion logic of the corresponding component signals could be recognized by Meyer, and because both Meyer and van der Wal disclosed the Altera FPGA (e.g. see fig.3 {Altera FPGA] in Meyer and col.30, lines 30-32 in van der Wal), which would have been suggested the use van der Wal into Meyer, which taught the use of same FPGA, in order to achieve the enhanced integration of the circuit components, and in doing so provided a motivation.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Rupp (5,784,636)) is cited for the basic teaching of the random access memory based FPGA (see figs.9,11, col.2, lines 12-60, col.3, lines 45-61, col.23, lines 60-67, col.24, lines 1-11, col.25, lines 5-47).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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